ASMEDIA TECHNOLOGY INC

ASM1442 Data Sheet

HDMI/DVI Level Shifter

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
1.0	February 4, 2009	Initial external release
1.1	Mar 19, 2009	Add description of RoHs
1.2	June 1, 2009	Update package information
1.3	Oct 22, 2009	Update marking information
1.4	June 18, 2010	Update pin description with pin#5 GND
1.5	Dec. 2, 2010	Add temperature spec
1.6	September 6, 2011	Update bandwidth support HDMI v1.4 in Features.
1.7	September 25, 2012	Update the feature description to support data transfer rate up to 3.4Gbps with the feature of Deep Color

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General Description

ASM1442 is the high speed TMDS level shift ICs for High Definition Multimedia Interface (HDMI) and Digital Video Interface (DVI) video application. Those convert low-swing AC-coupled differential input from existing PCI Express in the chipset of PC to HDMI compliant differential output, supporting up to 3.4Gbps bandwidth of pixel data transition, as indicated in HDMI Rev1.4a. This conversion is automatic and transparent to the user. The devices operate at a single 3.3V supply.

Application

- ◇ PC Motherboard
- ◇ Graphics Card
- ◇ Notebooks
- ◇ Docking Station

Features

- ◇ Coverts low-swing differential input to HDMI open-drain current steering Rx terminated differential output
- ◇ HDMI/DVI level shifting operation up to 3.4Gbps per lane
- ◇ Maximum data transfer rate conform with HDMI Revision 1.4a specification
- ◇ Supporting color depths greater than 24bits deep color mode
- ◇ Integrated 50Ω termination resistors for AC-coupled differential inputs.
- ◇ Enable/Disable feature to turn on/off TMDS inputs and outputs to enter low-power state.
- ◇ Output slew rate control on TMDS outputs to minimize EMI.
- ◇ Transparent operation: no re-timing or software configuration required.
- ◇ Integrated programmable receiving equalization.
- ◇ Integrated Hot Plug Detect (HPD) Inverting level shifter for ASM1442T.
- ◇ Integrated Hot Plug Detect (HPD) level shifter for ASM1442.
- ◇ Integrated pull-down resistor on HPD input guarantees "input LOW" when no display is plugged in.
- ◇ Integrated DDC level shifters, controlling by passgate through DDC_EN pin which allows 3.3V termination on PC chipset and 5V DDC termination on HDMI connector.
- ◇ DDC_EN function support.
- ◇ 3.3V±10% single power supply.
- ◇ ESD protection ability: HBM 4kV

Package Type

- ◇ 7x7 mm^2 QFN 48L
- ◇ Lead free, RoHs compliance.

Functional Diagram

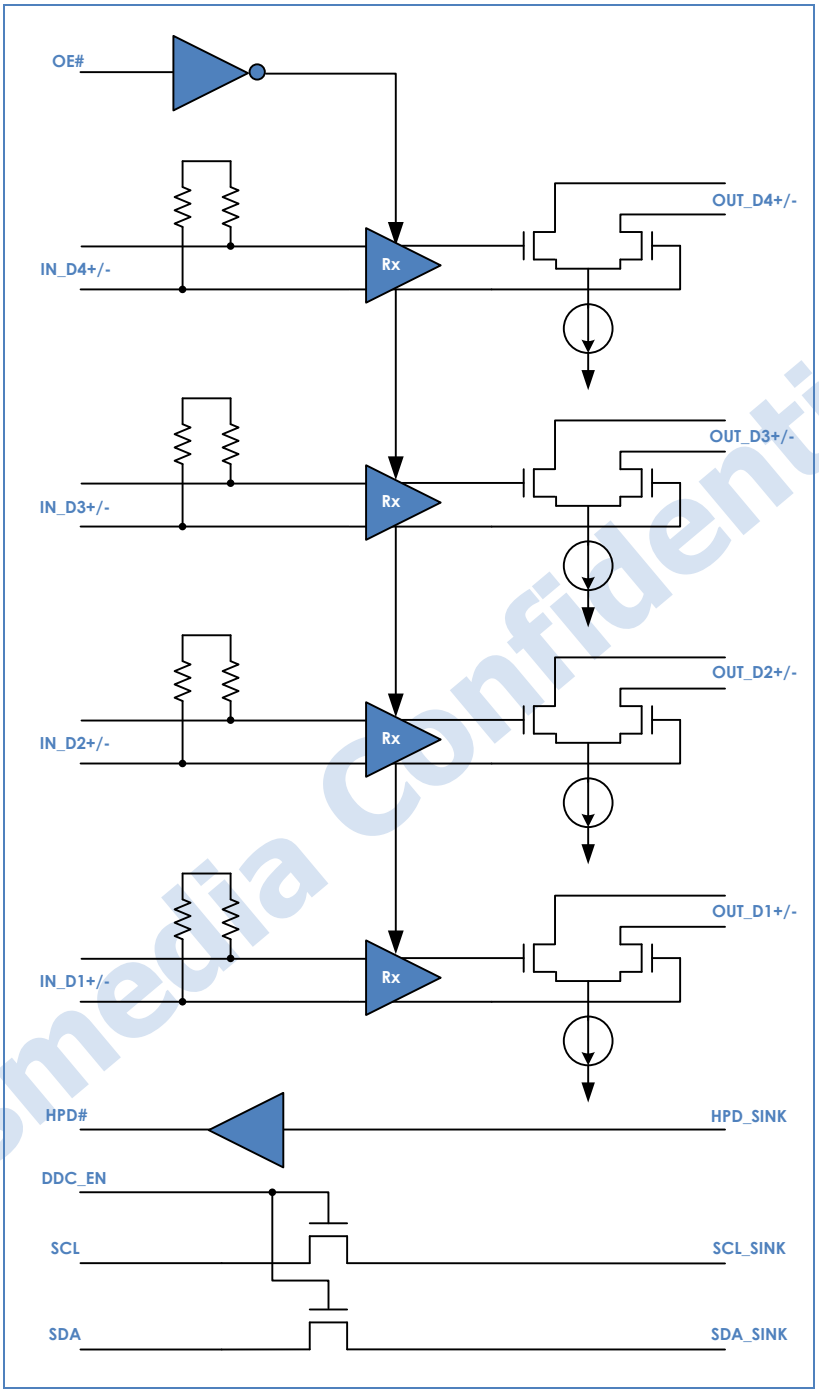


Figure 1: ASM1442 Functional Diagram

Application Examples

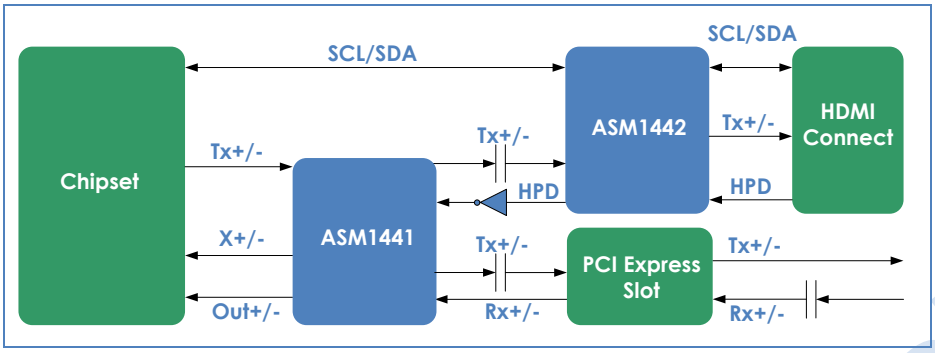


Figure 2: Application Example 1

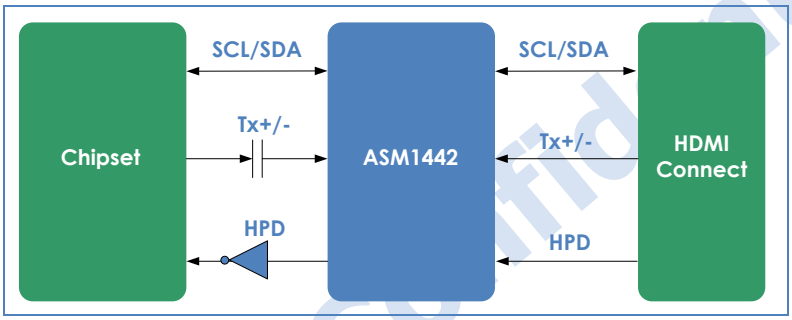


Figure 3: Application Example 2

Pinout Diagram

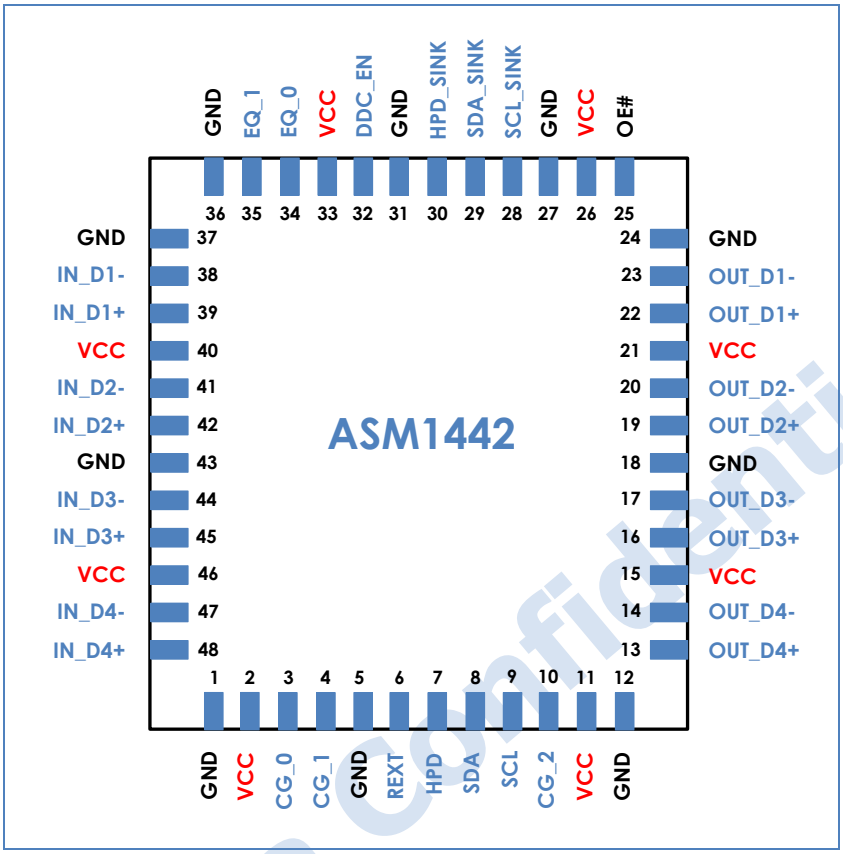


Figure 4: ASM1442 pinout

Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
P	Power pin
G	Ground pin
OD	Open Drain

Pin Name	Pin No.	Type	Descriptions
IN_D[4:1]-	47, 44, 41, 38	I	Negative singal of low-swing TMDS differential input from display source which output PCI Express electrical signaling with AC coupling signal.
IN_D[4:1]+	48, 45, 42, 39	I	Positive singal of low-swing TMDS differential input from display source which output PCI Express electrical signaling with AC coupling signal
OUT_D[4:1]-	14, 17, 20, 23	O	Negative singal of HDMI compliant TMDS differential output to display sink
OUT_D[4:1]+	13, 16, 19, 22	O	Positive singal of HDMI compliant TMDS differential output to display sink
HPD	7	O	Low frequency, 0V to 3.3V (nominal) output signal. Hot plug detection output to display source
HPD_SINK	30	I	Low frequency, 0V to 5V (nominal) input signal. This signal comes from the HDMI/DVI sink. If the voltage level of HPD_SINK goes high, it indicates "plugged" state; if the voltage level of HPD_SINK goes low, it indicates "unplugged". HPD_SINK is pulled down by an integrated pull down resistor.
SCL	9	OD	3.3V DDC Clock I/O connecting to display source. Pulled up by external termination to 3.3V. Connected to SCL_SINK through voltage-limiting integrated NMOS passgate internally.
SDA	8	OD	3.3V DDC Data I/O connecting to display source. Pulled up by external termination to 3.3V. Connected to SDA_SINK through voltage-limiting integrated NMOS passgate internally.
SCL_SINK	28	OD	5V DDC Clock I/O connecting to sink device. Pulled up by external termination to 5V. Connected to SCL through voltage-limiting integrated NMOS passgate.
SDA_SINK	29	OD	5V DDC Data I/O connecting to sink device. Pulled up by external termination to 5V. Connected to SDA through voltage-limiting integrated NMOS passgate.
OE#	25	I	Enable for level shifter path. OE#=1: IN_D[4:1]+/- high impedance, OUT_D[4:1]+/- high impedance OE#=0: IN_D[4:1]+/- is terminated 50Ω internally, OUT_D[4:1]+/- is Active Integrate internal pull-down resistor
DDC_EN	32	I	Enables the bias voltage to the DDC passgate level shifter gates. DDC_EN = 0V: passgate disabled DDC_EN = 3.3V: passgate enabled Integrate internal pull-up resistor
REXT	6	I	Connection to 3.4kΩ external resistor.
EQ_[1:0]	35, 34	I	Strapping Control pins are used to enable Input jitter elimination features. Refer to the table. Integrate internal pull-up resistor.

Pin Name	Pin No.	Type	Descriptions
CG_[2:0]	10, 4, 3	I	Strapping Control pins are used to enable output jitter elimination and control TMDS swing level. Refer to the table. Integrate internal pull-up resistor.
VCC	2, 11, 15, 21, 26, 33, 40, 46	P	3.3V±10% DC Power Supply
GND	1, 12, 18, 24, 27, 31, 36, 37, 43, 49	G	Ground

Strapping Table

TMDS Input Signal Equalization

EQ_1	EQ_0	Equalization	Note
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	Default

TMDS Output Signal Integrity

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note	
0	0	0	450	0	0		
0	0	1	420	0	-3dB	Shortest trace	
0	1	0	450	0	-3dB	Shortest trace	Default
0	1	1	460	0	-4dB		
1	0	0	340	0	0		
1	0	1	400	2dB	0	Longest trace	
1	1	0	400	2dB	0	Longest trace	
1	1	1	420	0	0		

Note: For the strapping setting of application, please refer to the application note.

Electrical Characteristics

Absolute Maximum Ratings

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Range	Unit
Power Supply	-0.5 ~ VCC+0.5	V
DC Input Voltage	-0.5 ~ VCC+0.5	V
Output Voltage	-0.5 ~ VCC+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

Electrical Characteristics (Recommended Operating Conditions)

Symbols	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	3.3V Power Supply		3.0	3.3	3.6	V
IDD	3.3V Supply Current	Total Current from VDD			100	mA
T	Operating temperature range		0		85	ºC
IOP	IDD @ Operating	Pixel clock=165MHz			100	mA
IPD	IDD @ Power Down	All control pins=low, except OE#			3	mA
TCASE	Case Temperature		0		85	^{0}C

Electrical Characteristics for IN_D[4:1]+/-

Symbols	Parameter	Min.	Nom.	Max.	Units	Comments
T_{BIT}	Unit Interval	360			ps	T_{BIT} is determined by the display mode. Nominal bit rate ranges from 250Mbps to 2.5Gbps per lane. Nominal T_{BIT} at 2.5Gbps = 400ps, 360ps = 400ps - 10%
$V_{RX-Diffp-p}$	Differential Input Peak to Peak Voltage	0.175		1.2	V	V_{RX-D+} = 2*| V_{RX-D+} - V_{RX-D-}|. Applies to IN_D and RX_IN signals.
T_{RX-EYE}	Minimum Eye Width at IN_D input pair	0.8			Tbit	The level shifter may add a maximum of 0.02UI jitter.
$V_{CM-AC-pp}$	AC Peak Common-Mode Input Voltage			100	mV	$V_{CM-AC-pp}$ = | V_{RX-D+} + V_{RX-D-}|/2 – $V_{CM-AC-DC}$. $V_{CM-AC-DC}$ = DC(avg) of | V_{RX-D+} + V_{RX-D-}|/2 $V_{CM-AC-pp}$ includes all frequencies above 30kHz.
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required IN_D+ as well as IN_D- DC impedance (50Ω ± 20% tolerance).
$V_{RX-Bias}$	Rx Input Termination Voltage	0		2.0	V	Intended to limit power-up stress on PCIE output buffers.
$Z_{RX-HIGH-Z}$	Single-end input resistance for IN_Dx when inputs are in high-Z state	100			kΩ	Differential inputs must be in a high impedance state.

Electrical Characteristics for OUT[4:1]+/-

Symbols	Parameter	Min.	Nom.	Max.	Units	Comments
V_H	Single-ended high level output voltage	AVCC – 10mV	AVCC	AVCC + 10mV	V	AVCC is the DC termination voltage in the HDMI or DVI Sink. AVCC is nominally 3.3V
V_L	Single-ended low level output voltage	AVCC – 600mV	AVCC – 500mV	AVCC – 400mV	V	The open-drain output pulls down from AVCC.
V_{SWING}	Single-ended output swing voltage	400	500	600	mV	Swing down from TMDS termination voltage (3.3V±10%)
I_{OFF}	Single-ended current in high-Z state			10	uA	Measured with TMDS outputs pulled up to AVCC Max (3.6V) through 50Ω resistors.
T_R	Rise Time	125		0.4T_{BIT}	ps	Maximum Rise/Fall time @ 2.7Gbps = 148ps. 125ps = 148 - 15%
T_F	Fall Time	125		0.4T_{BIT}	ps	Maximum Rise/Fall time @ 2.7Gbps = 148ps. 125ps = 148 - 15%
$T_{SKEW-INTRA}$	Intra-pair differential skew			10	ps	This differential skew budget is in addition to the skew presented between D+ and D- paired input pins.
$T_{SKEW-INTER}$	Inter-pair lane-to-lane output skew			250	ps	This lane-to-lane skew budget is in addition to the skew between differential input pairs.
T_{JIT}	Jitter added to TMDS signals			25	ps	Jitter budget for TMDS signals as they pass through the level shifter.

Electrical Characteristics for OE# and DDC_EN

Symbols	Parameter	Min.	Nom.	Max.	Units	Comments
V_{IH}	Input High Level	2.0		VDD	V	TMDS enable input changes state on cable plug/unplug.
V_{IL}	Input Low Level	0		0.8	V	
I_{IN}	Input Leakage Current			10	uA	Measured with input at V_{IHmax} and V_{ILmin}

Electrical Characteristics for HPD_SINK and HPD#

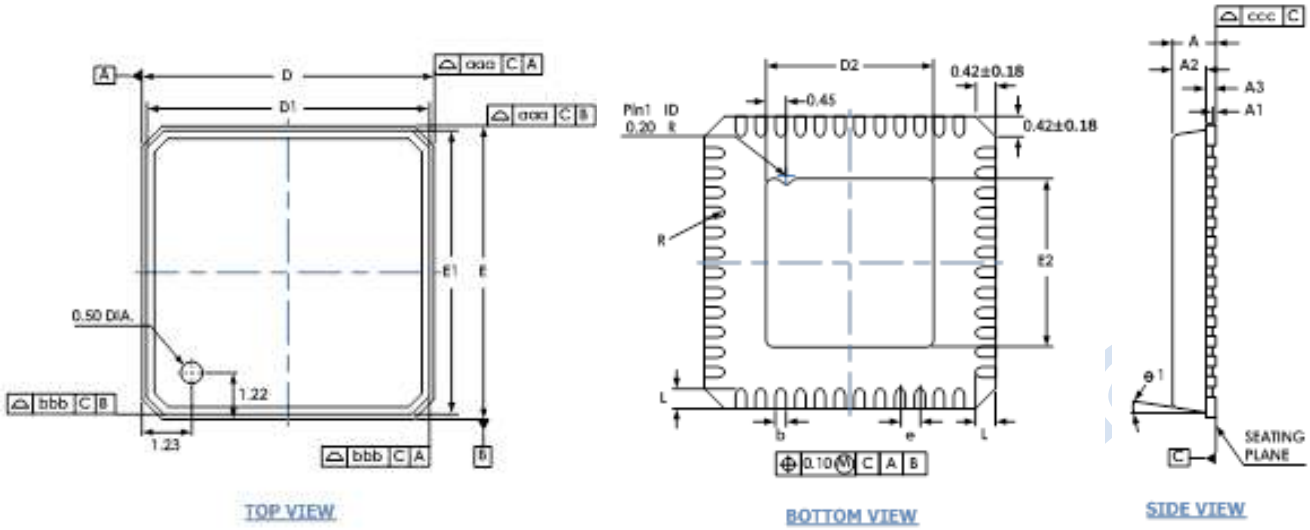
Symbols	Parameter	Min.	Nom.	Max.	Units	Comments
V_{IH-HPD_SINK}	HPD_SINK Input High Level	2	5	5.3	V	Low-speed input changes state on cable plug/unplug.
V_{IL-HPD_SINK}	HPD_SINK Input Low Level	0		0.8	V	
$I_{IN\_HPD\_SINK}$	HPD_SINK Input Leakage Current			50	uA	Measured with HPD_SINK at $V_{IH-HPD\_SINK\ max}$ and $V_{IL-HPD\_SINK\ min}$
$V_{OH-HPD\#}$	HPD# Output High-Level	3		3.6	V	For ASM1442 VCC = 3.3V ± 10%
		1.05		1.2	V	For ASM1442T VCC = 3.3V ± 10%
$V_{OL-HPD\#}$	HPD# Output Low-Level	0		0.2	V	
T_{HPD}	HPD_SINK to HPD# propagation delay			200	ps	Time from HPD_SINK changing state to HPD# changing state. Includes HPD# rise/fall time C_L = 10pF
T_{RF-HPD}	HPD# rise/fall time	1		20	ns	Time required to transition from $V_{OH-HPD\#}$ to $V_{OL-HPD\#}$ or

Symbols	Parameter	Min.	Nom.	Max.	Units	Comments
						from $V_{OL-HPD\#}$ to $V_{OH-HPD\#}$
R_{HPD}	HPD_SINK Input Pull-down Resistor	100	200	300	kΩ	Guarantees HPD_SINK is LOW when no display is plugged in.

Electrical Characteristics for SDA, SCL, SDA_SINK and SCL_SINK

Symbols	Parameter	Min.	Nom.	Max.	Units	Comments
V_{I-DDC}	Input Voltage	0		5.5	V	Voltage on DDC pins on connector end.
I_{LK-DDC}	Input Leakage			10	uA	V_I = 0V
C_I	Input / output capacitance			10	pF	
R_{ON}	Switch resistance			50	Ω	I_O = 3 mA, V_O = 0.4V

Package Information

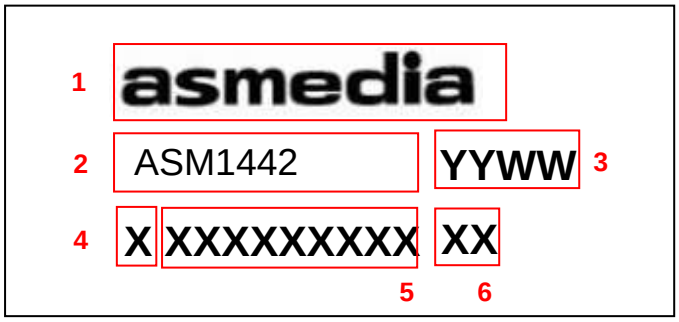


CONTROLLING DIMENSION : mm

Symbols	MILLIMETER			INCH		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.90	-	-	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	-	0.65	0.70	-	0.026	0.028
A3		0.20 REF.			0.008 REF.	
b	0.18	0.23	0.28	0.007	0.009	0.011
D		7.00 bsc			0.276 bsc	
D1		6.75 bsc			0.266 bsc	
D2	4.00	4.10	4.20	0.157	0.161	0.165
E		7.00 bsc			0.276 bsc	
E1		6.75 bsc			0.266 bsc	
E2	4.00	4.10	4.20	0.157	0.161	0.165
L	0.30	0.40	0.50	0.012	0.016	0.020
e		0.50 bsc			0.020 bsc	
θ1	0°	-	12°	0°	-	12°
R	0.075	-	-	0.003	-	-
Tolerances of Form and Position						
aaa		0.10			0.004	
bbb		0.10			0.004	
ccc		0.05			0.002	

Notes:
1. All dimensions are in millimeters.
2. Die thickness allowable is 0.305 mm maximum (0.012 inches maximum)
3. Dimensioning and tolerances conform to ASME Y14.5M. -1994.
4. Dimension applies to played terminal and is measured between 0.20 and 0.25 mm from terminal tip.
5. The pin#1 identifier must be placed on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. Package warpage max 0.08 mm.
8. Applied for exposed pad and terminals. Exclude embedding part of exposed pad from measuring.
9. Applied only to terminals.
10. Package corners unless otherwise specified are R0.175±0.025 mm.

Figure 5: Mechanical Specification – QFN 48L



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2. ASM1442: Product Name
3. YYWW: Date Code
4. X: Version of Marking Rule
5. XXXXXXXXX: Serial No. reserved for vendor
6. XX: Vendor Code